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Attorney for Applicant

Date: 23 April 2009

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.	:	**10/002,461**
Applicant	:	**SLAVIN, Keith R.**
Filed	:	**01 November 2001**
Titled	:	**Low Power, Hash-Content Addressable Memory Architecture**
Art Unit	:	**2189**
Examiner	:	**ELMORE, Reba I.**
Atty. Docket No.	:	**PAT000955-000 (013721-0110-999)**

APPELLANT'S REPLY BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Reply Brief is filed in response to the Examiner's Answer mailed 23 February 2009.

STATUS OF CLAIMS

Claims 41-44 are allowed.

The rejection of claims 4, 6-7, 11, 13-14, 18, 20-21, 24, 26-27, and 34-38 as being obvious over Hariguchi et al. (U.S. 6,665,297) in view of Cheriton (U.S. 7,002,965) has been withdrawn. Those claims are believed to be in condition for allowance over the art of record.

Claims 1-38 stand rejected under 35 U.S.C. § 112 first paragraph.

Claims 1-3, 5, 8-10, 12, 15-17, 19, 22-23, 25, and 28-33 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hariguchi et al. in view of Cheriton.

ARGUMENT

A. The rejection of claims 1-3, 6-10, 12-17, 19-23, and 25-33 under 35 U.S.C. § 112, first paragraph, is improper and should be reversed.

The delay element does not appear in claims 1-3, 6-10, 12-17, 19-23, and 25-33. In section 10 (Response to Argument) of the Answer, the examiner states that the delay circuit "appears to be very important." The examiner also states that the delay circuit "appears to be necessary." Finally, the examiner asserts that "the delay circuit is essential subject matter as it is in the claims." There is no evidence in this record to support the Office's bald assertion that the delay element is essential subject matter, and therefore, even though not recited in claims 1-3, 6-10, 12-17, 19-23, and 25-33, the delay element should have been.

The examiner's assertion (that because the delay element appears in claim 4, the delay element is essential subject matter) is not supportable. There is no case law to support the argument that just because an element appears in a dependent claim, that element is essential subject matter with respect to all the claims. In fact, the recitation of an element in a dependent claim is evidence that the inventor believed that element to be non-essential with respect to the dependent claim's base claim. The recitation of the delay element in claim 4 may not be relied upon as a basis to support the assertion that the delay element is essential subject matter of claim 1.

The only argument put forth by the examiner to support the assertion that the delay element is essential subject matter is the argument that there is allegedly no embodiment in the present disclosure that does not use the delay element. That is not true. In the description of the preferred embodiment found in paragraph [0021], the following statement appears:

> The TCAM 20 also receives the small n-bit comparand word which <u>may be</u> input to the TCAM 20 through a delay circuit 28. (Emphasis added.)

The use of the permissive language <u>may be</u> clearly indicates that the use of the delay circuit is not essential, mandatory, or important. Furthermore, the summary of the invention does not mention the delay element. If the examiner's assertion that the delay element is an essential subject matter is true, then one would expect a description of the delay element to appear in the summary of the invention. It is clear that if the specification is objectively viewed,

there is no indication in the specification to support the examiner's assertion that the delay element is essential subject matter.

Additionally, it is quite apparent that the delay element can be eliminated if the comparand word is presented to the TCAM in a persistent manner.

Applicant has set forth the subject matter which applicant wishes to claim in claims 1-3, 6-10, 12-17, 19-23, and 25-33. On this record, the Office has no basis for asserting that any critical, essential, or important subject matter has been omitted from those claims. Therefore, the rejection of claims 1-3, 6-10, 12-17, 19-23, and 25-33 should be reversed.

B. The rejection of claims 4, 5, 11, 18, 24, and 34-38 under U.S.C. § 112, first paragraph, is utterly unsupported.

The examiner acknowledges that a delay circuit per se may be known. See Examiner's Answer, page 9, lines 7-8. Remarkably, however, by indicating in the specification what signal is to be delayed, and how long the delay should be, that disclosure somehow renders such known delay circuits incapable of being implemented. If delay circuits per se are known, and the specification and claims indicate what signal is to be input and how long the delay should be for, what else do you need to tell a person of ordinary skill in the art? Applicant respectfully notes that specifications are written for persons of ordinary skill in the art and preferably omit details that are well known to such persons. *Genetech, Inc. v. Novo Nordisk A/S*, 108 F.3d 1361 (Fed. Cir. 1997).

While the examiner has attempted to support this ground of rejection by raising a number of questions, there is no *evidence* in this record that all of the examiner's questions could not be easily answered by a person of ordinary skill in the art. The examiner's statement on page 10 that the delay circuit is being used "in a very specific way" in the present invention is misleading. It is true that the applicant is using the delay circuit to delay a *specific signal* (the comparand word) for a *specific period of time* (until the TCAM is precharged), but the delay circuit is doing nothing more than delaying what is input to it for a predetermined period of time. It is not understood how a specification becomes non-enabling by telling a person of ordinary skill in the art what signal is to be input to any known prior art delay circuit and for how long that signal is to be delayed. That seems to be precisely the information, and all the information, that a person

of ordinary skill in the art needs to implement the delay circuit. Applicant is prepared to rebut any *evidence* the Office may have to support this ground of rejection, but applicant cannot rebut what appears to be the examiner's subjection belief.

Finally, the examiner's continued reliance on *Automotive Technologies International, Inc. v. BMS of North America, Inc.*, 501 F.3d 1274 (Fed. Cir. 2007) is surprising inasmuch as the examiner acknowledges that many of the factors in that case, factors that caused the court to rule as it did, are *not present* in this case. Applicant reiterates the following differences between *Automotive Technologies International* and the present case which makes *Automotive Technologies International* inapplicable here:

- That case involved a situation where a mechanical side impact sensor was disclosed in detail but the claims recited an electronic side impact sensor. There is no dichotomy in the instant application between what is disclosed and what is claimed. And what is claimed is claimed in no more detail than what is disclosed. (The examiner acknowledges that applicant is not trying to claim more than what is disclosed.) (See Examiner's Answer, page 10, line 1.)
- The court in that case stated that "the novel aspect of this invention is using a velocity-type sensor for side impact sensing." Thus, the specification in the case cited by the examiner was silent precisely at the "point of novelty." (The examiner stated that the delay element was essential because there was no embodiment without the delay element but ignored the permissive language used in the specification and the fact that the summary of the invention does not mention the delay element.)
- The specification in the case cited by the examiner stated that side impact sensing is a new field. There is no corresponding statement in this case that the construction of delay circuits is a new field. (The examiner conceded this point in her answer.) (See page 10, lines 3-4.)
- The court had testimony that indicated that a "great deal of experimentation" would have been necessary to make an electronic side impact sensor after reading the specification in the case cited by the examiner. There is no evidence in this record that a great deal of experimentation would be necessary to construct a delay circuit.

(The examiner conceded this point in her answer.) (See page 10, lines 5-8.)

For the foregoing reasons, it is respectfully requested that the rejection of claims 1-38 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement, be reversed.

C. The rejection of claims 1-3, 5, 8-10, 12, 15-17, 19, 22-23, 25, and 28-33 as being obvious over Hariguchi et al. (U.S. Patent No. 6,665,297 "Hariguchi") in view of Cheriton (U.S. Patent No. 7,002,865) is not supported by the teachings of the references and should be reversed.

On the bottom of page 5 of the Examiner's Answer, the examiner argues that "enabling or precharging portions of a CAM in response signals [*sic*] as portions of the CAM being enabled when an input is sent to the CAM" is taught by Hariguchi at Column 7, line 50 to Column 8, line 3. That portion of Hariguchi provides, in the context of Figure 5 of Hariguchi, as follows:

> During a third pipeline clock cycle, in the selection stage 88, a priority encoder 170 identifies the output pointer associated with the longest match among the hash circuits 82 (FIG. 2) and CAM 80. The priority encoder 170 receives the hash circuit hit/miss flags (H/M/32 . . . H/M/8) from the hash circuits 82 (FIG. 2) and the CAM hit/miss (H/M) flag from the CAM 80. The priority encoder 170 also receives the prefix length of the match from the CAM 80. The hit/miss flags from each hash bucket circuit are input to predetermined lines of the priority encoder 170 such that each line corresponds to the unmasked prefix length of that hash bucket circuit. In the priority encoder 170, a hash match register 171 includes a hash hit/miss flag, a matching hash address, and the matched hash prefix length. When the CAM 80 has the prefix length indicating the longest match, the priority encoder 170 outputs a CAM/hash select signal indicating the CAM. When one of the hash circuits has the longest match, the priority encoder 170 outputs a CAM/hash select signal indicating the hash circuits and also outputs a longest match select code signal corresponding to the hash circuit having the longest match.

There is no teaching of enabling the CAM or of enabling a portion of a CAM in this section of Hariguchi.

On page 6 of the Examiner's Answer, at lines 13-14, the Office concedes:

> . . . the primary reference does not specifically teach using hash signals to enable portions of a CAM.

The examiner must rely on the secondary reference, Cheriton, for a teaching of "using a hash function to enable portions of a CAM," and cites Figure 3, and Column 6, line 43 to Column 7, line 21, reproduced below to support the Office's position.

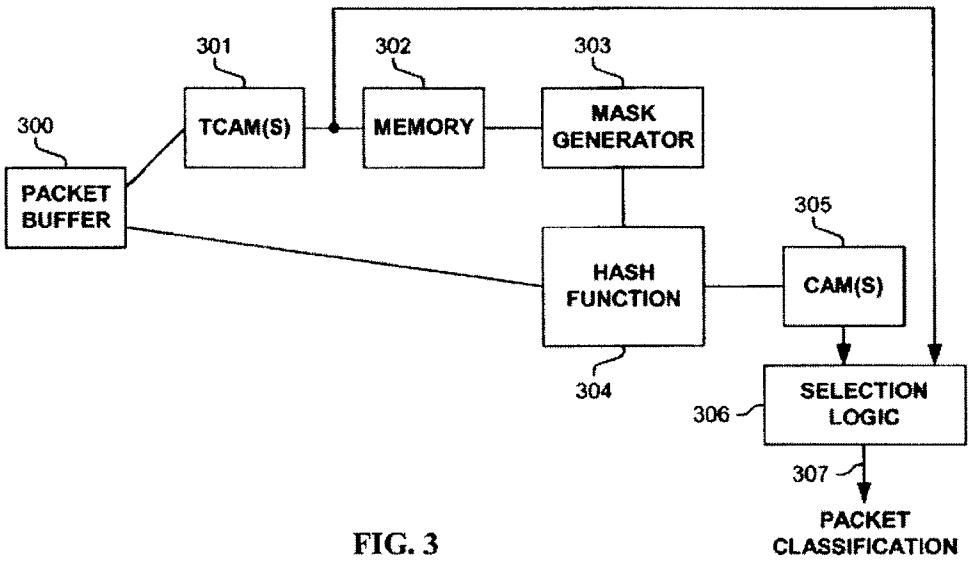


FIG. 3

FIG. 3 illustrates a block diagram of one exemplary embodiment including one or more TCAMs 301 for handling input and output classification (e.g., for ACLs, QoS, NAT, encryption, etc.) for a packet or packet header stored in packet buffer 300. This illustrated embodiment also includes one or more forwarding CAMs 305 to classify packets for IP forwarding decisions.

On packet reception, the packet flow label is extracted from the received

packet and passed to the classification TCAMs 301. In one embodiment, TCAMs 301 typically accept a full flow label including IP source and destination addresses, protocol type, flags and layer 4 source and destination ports, a virtual local area network (VLAN) id and/or other fields. The system includes a hash directory of flow labels implemented in a large SRAM memory 302, suitable for flow classification for netflow statistics, microflow policing and redirection. Using on-chip SRAM, this hash directory may be implemented, for example, as a 16-set associative hash table, effectively implementing a binary associative memory. In one embodiment, TCAMs 301 produce an index which is used by classification memory 302 to return an entry that provides indications on forwarding, policing and/or other packet classification indications.

In one embodiment, the full flow label of the packet is then masked off by mask generator 303. A mask is typically selected based on other classifications applied to the packet, including classification produced by TCAM 301. The masked flow label is then used as the hashing key, and a lookup operation is performed in the hash directory using this mask in hash function 304. In one embodiment, a CAM or other lookup structure (e.g., TRIE) is used in place or, or in addition to the hash table. If a matching hash directory entry is found by hash function 304, the handling specified by this directory entry is used by one or more CAMs 305 to generate one or more classification indications and overriding the relevant handling that may have been determined by earlier packet classification mechanisms. If the one or more CAMs 305 may generate multiple classification indications, selection logic 306 is used to select between the classification indications, and to generate the packet classification 307. Additionally, selection logic 306 may further receive and use the result of generated by TCAMs 301 in making its selection. For example, in one embodiment, TCAMs 301 may generate a forwarding and/or policing decision, and CAMs 305 may be used to override this generated forwarding and/or policing decision. (Emphasis added).

Cheriton in no way teaches using a hash function to enable or even to choose portions of a CAM.

The examiner relies on the language of Column 7, lines 7-12, emphasized above, to argue on page 10, lines 12-14, of the Examiner's Answer that because "the results of the hash directory match is used by one or more CAMs" that is a teaching of "enabling the CAM using the hash function output." The examiner is reading knowledge of the claimed invention onto the prior art because the words of Cheriton neither say nor suggest any teaching of *enabling* or *precharging* the CAM using the hash function output.

The examiner continues the explanation of Cheriton on page 10, lines 17-21, of the Examiner's Answer as follows:

> Cheriton teaches enabling at least a portion of the CAM at column 7, lines 9-10, where it is taught that the hash entry is used to generate "one or more classification indications" (where "one" classification indication at least reads on the claimed "portion"). In either condition, the CAM addresses are enabled in direct response to the output of the hash directory of the Cheriton reference.

It is respectfully submitted that the examiner is again reading knowledge of the claimed invention onto the prior art because the words of Cheriton neither say nor suggest any teaching of *enabling* or *precharging* the CAM using the hash function output nor do the words of Cheriton say or suggest enabling or precharging *one of several* CAMs 305 (only one CAM 305 is illustrated in the figure).

This ground of rejection must be reversed.

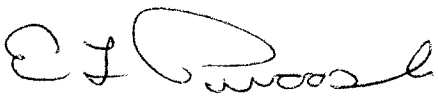
D. The rejection of claims 5, 12, 19, and 25 as being obvious over Hariguchi in view of Cheriton is incorrect and should be reversed.

Each of the dependent claims 12, 19, and 25 recites precharging *portions* of the CAM while claim 5 recites enabling portions of the CAM. The examiner cites Column 4, line 63 to Column 5, line 14, of Hariguchi as teaching this limitation. The cited portion of Hariguchi is the description of the router 26 and router control procedure. There is no disclosure in that portion, or any other portion, of Hariguchi that teaches precharging/enabling *portions* of a CAM. In addition, this ground of rejection is inconsistent with page 7 of the Office action in which the examiner indicates that Hariguchi, the primary reference, "does not specifically teach using hash signals to enable portions of a CAM." Accordingly, the rejection of claims 5, 12, 19, and 25 should be reversed.

CONCLUSION

For the foregoing reasons, it is respectfully requested that the rejection of all of the claims be reversed.

Respectfully submitted,



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